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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,814	09/18/2003	Ramakrishnan Rajamony	AUS920030528US1	8944

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EXAMINER	
BAKER, PAUL A	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,814	RAJAMONY ET AL.	
	Examiner	Art Unit	
	Paul A. Baker	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 12-17* is/are rejected.

7)☒ Claim(s) *9-11 and 18-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6,8 and 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Runas, US Patent 5,506,810.

In regards to claim 1, Runas discloses a memory controller in figure 2A, comprising:

an access control circuit for providing control signals to a memory (element 205),

wherein said access control circuit has a selectable page mode for controlling a held-open state of a selected row within said memory after an access is complete (mode select signal and column 4 line 67 through column 5 line 5); and

a counter circuit coupled to said access control circuit for counting consecutive accesses to said selected row and further coupled to a control input of said access control circuit whereby said selectable page mode is set in conformity with a result of said counting, whereby an average latency of said memory is for access, and whereby rows of said memory are selected reduced (element 212, 207, figure 2B /RAS only asserted once, eliminating subsequent associated /RAS delays).

In regards to claim 2, Runas discloses said selectable page mode includes a page count mode for holding said selected row open for a number of accesses equal to a count value in column 5 lines 38-41 and lines 52-59, column 6 lines 2-9.

In regards to claim 3, Runas discloses said counter circuit comprises a first counter for determining said count value by counting a number of consecutive accesses for which said selected row is selected (figure 2A element 212), and a control logic for holding said selected row open for a number of accesses determined in conformity with said first number of consecutive accesses (figure 2A elements 211, 215).

In regards to claim 4, Runas discloses said counter circuit comprises a second counter for counting a next number of consecutive accesses for which another row is selected subsequent to completion of said first counter counting a first group of consecutive accesses to said selected row in figure 2A element 209.

In regards to claim 5, Runas discloses a comparison logic coupled to said first counter and said second counter for validating that said next number of consecutive accesses is equal to said first number of consecutive accesses in column 6 lines 2-5.

In regards to claim 6, Runas discloses said first counter, said second counter and said comparison logic form a state machine for controlling said number of accesses for

which said row held open in figure 2A element 205, evidenced by functionality disclosed in column 5 line 60 through column 6 line 23.

In regards to claim 8, Runas discloses said counter circuit comprises:

a first counter coupled to said access control circuit for determining a number of consecutive accesses for which said selected row is selected (figure 2A element 212) and a second counter coupled to said access control circuit for counting a total number of accesses to said memory (figure 2A element 209).

In regards to claim 12, Runas discloses said access control circuit closes said row by issuing a precharge command in response to assertion of said control input by said counter circuit in column 6 lines 37-49.

In regards to claim 13, Runas discloses a memory device, comprising:

a plurality of storage cells arranged by columns and rows in figure 2A elements 203 and 204;

control logic (figure 2A element 205) for accessing one of said storage cells by precharging a plurality of column bitlines each coupled to a unique member of each row, selecting an entire row for output to said column bitlines, and selecting a column for output (figure 2A elements 213a and 213b), wherein said control logic includes a selectable page mode for selectively disabling said row and precharging said column

bitlines in anticipation of access to another row (figure 2A, mode select signal controlling 215 in turn controlling element 211); and

a counter circuit coupled to said control logic for counting consecutive accesses to said selected row and further coupled to a control input of said control logic, wherein said selectable page mode is set in conformity with a result of said counting (figure 2A element 212 and 211 controlled by 215), whereby an average latency of said memory device is reduced (figure 2B /RAS only asserted once, eliminating subsequent associated /RAS delays).

In regards to claim 14, Runas discloses said selectable page mode includes a page count mode for holding said selected row open for a number of accesses equal to a count value in column 5 lines 38-41 and lines 52-59, column 6 lines 2-9.

In regards to claim 15, Runas discloses a method of managing reads in a memory array, comprising:

first counting a number of consecutive row accesses to a first row of said memory array (in figure 2A element 212); and

in conformity with a result of said counting, selecting a page mode of said memory array (figure 2A mode select signal), wherein a last-accessed row of said memory is held open subsequent to accesses to said row (in column 5 lines 38-41 and lines 52-59, column 6 lines 2-9), whereby an average latency of said memory array is

reduced (figure 2B /RAS only asserted once, eliminating subsequent associated /RAS delays).

In regards to claim 16, Runas discloses said selecting further sets a count said page mode, and wherein said method further comprises second counting consecutive accesses to a second row of said memory array and wherein said last-accessed row is held open only while a second count of said second counting is less than said count of said page mode (figure 2A element 209, column 6 lines 2-5).

In regards to claim 17, Runas discloses third counting consecutive accesses to another row of said memory array, subsequent to said first counting;

comparing a third count of said third counting to a first count of said first counting; and

in response to said comparing determining that said first count and said third count are equal, setting said count of said page mode to said first count (column 6 lines 5-23, column 6 line 56 through column 7 lines 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Runas, US Patent 5,506,810.

In regards to claim 7, Runas does not disclose a control register for setting said count value, whereby said counter circuit is programmed to count down a number of consecutive access cycles for which said row is held open.

It is well known in the art there are three methods for counting consecutive memory addresses within a row, the first as disclosed by Runas is the comparison of a real address value contained within the counter with a final real address value wherein the counter is incremented between consecutive addresses, the second is the comparison of an offset value contained within the counter with a final offset value wherein the counter is incremented between consecutive addresses, the third as claimed by applicant is a count of remaining addresses which is compared with the value 0 wherein the counter is decremented between consecutive addresses. The first two methods require comparison of the counter value with a non-zero value, this requires non-trivial comparison logic and a register to store the final value. The third method requires a trival comparison logic comprised of a $\log_2$(row length) input NAND gate of the counter value, and no register. The reduction of logic complexity with the third method requires less silicon space resulting in less cost for manufacturer, therefore it would have been obvious to one of ordinary skill in the art at the time of invention to replace Runas' disclosed method of counting consecutive column addresses within a

row with the third method of counting down a predetermined number of locations within the row.

Allowable Subject Matter

Claims 9-11, 18-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Baker whose telephone number is (571)272-4203. The examiner can normally be reached on M-F 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Mano Padmanabhan
4/14/05

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PB